

WHAT IS CLAIMED IS:

1 1. For use in a receiver, a round off mechanism for
2 maintaining a mean value of an operand comprising:

3 an incrementer selectively incrementing said
4 operand at a most significant discard bit position to
5 generate an incremented intermediate rounding result; and

6 control logic controlling an output of said round
7 off mechanism, said control logic causing said round off
8 mechanism to produce a rounded result equal to either

9 a remainder of said operand after truncation
10 of bits within selected discard bit positions within
11 said operand, said selected discard bit positions
12 including said most significant discard bit position,
13 or
14

15 a remainder of said incremented intermediate
16 rounding result after truncation of bits within said
17 selected discard bit positions within said incremented
 intermediate result.

1 2. The round off mechanism as set forth in Claim 1
2 wherein said control logic causes said round off mechanism
3 to produce:

4 said remainder of said operand after truncation
5 of said bits within said selected discard bit positions as
6 said rounded result when said operand is

7 positive, or

8 negative and contains a logical one within
9 said most significant discard bit position and at
10 least one other bit position within said selected
11 discard bit positions; and

12 said remainder of said incremented intermediate
13 rounding result after said truncation of said bits within
14 said selected discard bit positions as said rounded result
15 when said operand is negative and contains

16 a logical zero within said most significant
17 discard bit position, or

18 a logical one within said most significant
19 discard bit position and logical zeros in any
20 remaining discard bit positions.

1 3. The round off mechanism as set forth in Claim 1
2 wherein said control logic causes said round off mechanism
3 to select between

4 said remainder of said operand after
5 truncation of said bits within said selected discard
6 bit positions, and

7 said remainder of said incremented
8 intermediate rounding result after said truncation of
9 said bits within said selected discard bit positions
10 as said rounded result.

11 4. The round off mechanism as set forth in Claim 1
12 wherein said round off mechanism avoids any offset within
13 said rounded result.

1 5. The round off mechanism as set forth in Claim 1
2 wherein said round off mechanism computes both said
3 remainder of said operand after truncation of said bits
4 within said selected discard bit positions and said
5 remainder of said incremented intermediate rounding result
6 after said truncation of said bits within said selected
7 discard bit positions for said operand,

8 wherein said control logic causes said round off
9 mechanism to select

10 said remainder of said operand after truncation
11 of said bits within said selected discard bit positions as
12 said rounded result when said operand is

13 positive, or

14 negative and contains a logical one within
15 said most significant discard bit position and at
16 least one other bit position within said selected
17 discard bit positions, and

18 said remainder of said incremented intermediate
19 rounding result after said truncation of said bits within
20 said selected discard bit positions as said rounded result
21 when said operand is negative and contains

22 a logical zero within said most significant
23 discard bit position, or

24 a logical one within said most significant
25 discard bit position and logical zeros in any
26 remaining discard bit positions.

PHIL06-01438

1 6. A receiver comprising:

2 a computation unit;

3 a round off mechanism receiving an operand from
4 said computation unit and maintaining a mean value of said
5 operand during rounding, said round off mechanism
6 comprising:

7 an incrementer selectively incrementing said
8 operand at a most significant discard bit position to
9 generate an incremented intermediate rounding result;
10 and

11 control logic controlling an output of said
12 round off mechanism, said control logic causing said
13 round off mechanism to produce a rounded result equal
14 to either

15 a remainder of said operand after
16 truncation of bits within selected discard bit
17 positions within said operand, said selected
18 discard bit positions including said most
19 significant discard bit position, or

20 a remainder of said incremented
21 intermediate rounding result after truncation of
22 bits within said selected discard bit positions
23 within said incremented intermediate result.

1 7. The receiver as set forth in Claim 6 wherein said
2 control logic causes said round off mechanism to produce:

3 said remainder of said operand after truncation
4 of said bits within said selected discard bit positions as
5 said rounded result when said operand is

6 positive, or

7 negative and contains a logical one within
8 said most significant discard bit position and at
9 least one other bit position within said selected
10 discard bit positions; and

11 said remainder of said incremented intermediate
12 rounding result after said truncation of said bits within
13 said selected discard bit positions as said rounded result
14 when said operand is negative and contains

15 a logical zero within said most significant
16 discard bit position, or

17 a logical one within said most significant
18 discard bit position and logical zeros in any
19 remaining discard bit positions.

1 8. The receiver as set forth in Claim 6 wherein said
2 control logic causes said round off mechanism to select
3 between

4 said remainder of said operand after
5 truncation of said bits within said selected discard
6 bit positions, and

7 said remainder of said incremented
8 intermediate rounding result after said truncation of
9 said bits within said selected discard bit positions
10 as said rounded result.

1 9. The receiver as set forth in Claim 6 wherein said
2 round off mechanism avoids any offset within said rounded
3 result.

1 10. The receiver as set forth in Claim 6 wherein said
2 round off mechanism computes both said remainder of said
3 operand after truncation of said bits within said selected
4 discard bit positions and said remainder of said
5 incremented intermediate rounding result after said
6 truncation of said bits within said selected discard bit
7 positions for said operand,

8 wherein said control logic causes said round off
9 mechanism to select

10 said remainder of said operand after truncation
11 of said bits within said selected discard bit positions as
12 said rounded result when said operand is

13 positive, or

14 negative and contains a logical one within
15 said most significant discard bit position and at
16 least one other bit position within said selected
17 discard bit positions, and

18 said remainder of said incremented intermediate
19 rounding result after said truncation of said bits within
20 said selected discard bit positions as said rounded result
21 when said operand is negative and contains

22 a logical zero within said most significant
23 discard bit position, or

24 a logical one within said most significant
25 discard bit position and logical zeros in any
26 remaining discard bit positions.

1 11. For use in a receiver, a method of maintaining a
2 mean value of an operand during rounding comprising:

3 selectively incrementing the operand at a most
4 significant discard bit position to generate an incremented
5 intermediate rounding result; and

6 producing a rounded result equal to either

7 a remainder of the operand after truncation
8 of bits within selected discard bit positions within
9 the operand, the selected discard bit positions
10 including the most significant discard bit position,
11 or
12

13 a remainder of the incremented intermediate
14 rounding result after truncation of bits within the
15 selected discard bit positions within the incremented
16 intermediate result.

1 12. The method as set forth in Claim 11 wherein the
2 step of producing a rounded result further comprises:

3 producing the remainder of the operand after
4 truncation of the bits within the selected discard bit
5 positions as the rounded result when the operand is

6 positive, or

7 negative and contains a logical one within
8 the most significant discard bit position and at least
9 one other bit position within the selected discard bit
10 positions; and

11 producing the remainder of the incremented
12 intermediate rounding result after the truncation of the
13 bits within the selected discard bit positions as the
14 rounded result when the operand is negative and contains

15 a logical zero within the most significant
16 discard bit position, or

17 a logical one within the most significant
18 discard bit position and logical zeros in any
19 remaining discard bit positions.

1 13. The method as set forth in Claim 11 wherein the
2 step of producing a rounded result further comprises:

3 selecting between the remainder of the operand
4 after truncation of the bits within the selected discard
5 bit positions and the remainder of the incremented
6 intermediate rounding result after the truncation of the
7 bits within the selected discard bit positions.

1 14. The method as set forth in Claim 11 wherein the
step of producing a rounded result avoids any offset within
the rounded result.

1 15. The method as set forth in Claim 11 wherein the
2 step of producing a rounded result further comprises:

3 computing both the remainder of the operand after
4 truncation of the bits within the selected discard bit
5 positions and the remainder of the incremented intermediate
6 rounding result after the truncation of the bits within the
7 selected discard bit positions for the operand;

8 selecting the remainder of the operand after
9 truncation of the bits within the selected discard bit
10 positions as the rounded result when the operand is

11 positive, or

12 negative and contains a logical one within
13 the most significant discard bit position and at least
14 one other bit position within the selected discard bit
15 positions; and

16 selecting the remainder of the incremented
17 intermediate rounding result after the truncation of the
18 bits within the selected discard bit positions as the
19 rounded result when the operand is negative and contains

20 a logical zero within the most significant
21 discard bit position, or

22 a logical one within the most significant
23 discard bit position and logical zeros in any
24 remaining discard bit positions.

1 16. A computer program product within a computer
2 usable medium for maintaining a mean value of an operand
3 during rounding comprising:

4 instructions for selectively incrementing the
5 operand at a most significant discard bit position to
6 generate an incremented intermediate rounding result; and

7 instructions for producing a rounded result equal
8 to either

9 a remainder of the operand after truncation
10 of bits within selected discard bit positions within
11 the operand, the selected discard bit positions
12 including the most significant discard bit position,
13 or

14 a remainder of the incremented intermediate
15 rounding result after truncation of bits within the
16 selected discard bit positions within the incremented
17 intermediate result.

1 17. The computer program product as set forth in
2 Claim 16 wherein the instructions for producing a rounded
3 result further comprise:

4 instructions for producing the remainder of the
5 operand after truncation of the bits within the selected
6 discard bit positions as the rounded result when the
7 operand is

8 positive, or

9 negative and contains a logical one within
10 the most significant discard bit position and at least
11 one other bit position within the selected discard bit
12 positions; and

13 instructions for producing the remainder of the
14 incremented intermediate rounding result after the
15 truncation of the bits within the selected discard bit
16 positions as the rounded result when the operand is
17 negative and contains

18 a logical zero within the most significant
19 discard bit position, or

20 a logical one within the most significant
21 discard bit position and logical zeros in any
22 remaining discard bit positions.

1 18. The computer program product as set forth in
2 Claim 16 wherein the instructions for producing a rounded
3 result further comprise:

4 instructions for selecting between the remainder
5 of the operand after truncation of the bits within the
6 selected discard bit positions and the remainder of the
7 incremented intermediate rounding result after the
8 truncation of the bits within the selected discard bit
9 positions.

10 19. The computer program product as set forth in
11 Claim 16 wherein the instructions for producing a rounded
12 result avoid any offset within the rounded result.

1 20. The computer program product as set forth in
2 Claim 16 wherein the instructions for producing a rounded
3 result further comprise:

4 instructions for computing both the remainder of
5 the operand after truncation of the bits within the
6 selected discard bit positions and the remainder of the
7 incremented intermediate rounding result after the
8 truncation of the bits within the selected discard bit
9 positions for the operand;

10 instructions for selecting the remainder of the
11 operand after truncation of the bits within the selected
12 discard bit positions as the rounded result when the
13 operand is

14 positive, or

15 negative and contains a logical one within
16 the most significant discard bit position and at least
17 one other bit position within the selected discard bit
18 positions; and

19 instructions for selecting the remainder of the
20 incremented intermediate rounding result after the
21 truncation of the bits within the selected discard bit
22 positions as the rounded result when the operand is
23 negative and contains

24 a logical zero within the most significant
25 discard bit position, or
26 a logical one within the most significant
27 discard bit position and logical zeros in any
28 remaining discard bit positions.